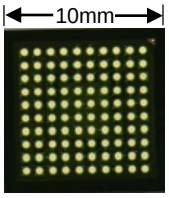
Micro-RDC
Microelectronics Research Development Corporation

Radiation Hardened By Design Parallel to SPI NV Memory Interface (KM-803310)

Feature Sheet

Supports the following functions:

- **Parallel to SPI Non-volatile Memory Interface**
- **SPI to 128x8 Register File; SEU Immune**



10x10 0.8 mm Pitch BGA

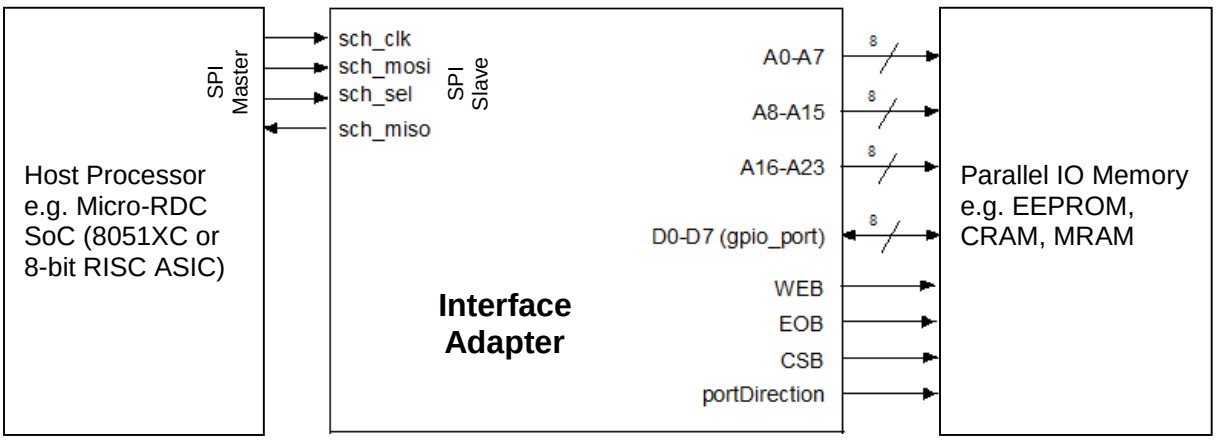
Manufactured using IBM's 90nm Low Power CMOS Process, using Micro-RDC Radiation-Hardened-By-Design (RHBD) Technology:

- Radiation Hardness (MIL-STD 883)
  - TID>1 Mrad(Si)
  - SEL immune > 75 MeV-cm2/mg (LET)
  - Patented Temporal Latch: Provides SET immunity to pulse widths up to 1ns
- Operating range – Voltages: 1.2V to 2.5V IO*; 1.2V Core; Temperature: -55ºC to +125ºC
- Clock: DC to 50 MHz

  * Maximum IO voltage may increase pending characterization in progress

Parallel to SPI Nonvolatile Memory Interface Features

- SPI Slave to Parallel NVM Interface Support
- 24 bit Address to Parallel NVM
- 8 bit Bidirectional Bus to Parallel NVM
- Handshake to Parallel NVM
- On-chip Rad Hard temporal latch register file (128x8)
- SPI to 8-bit Bi-directional GPIO
- IO Expansion
- Compatible with Northrup Grumman EEPROM, BAE CRAM and Honeywell NVM



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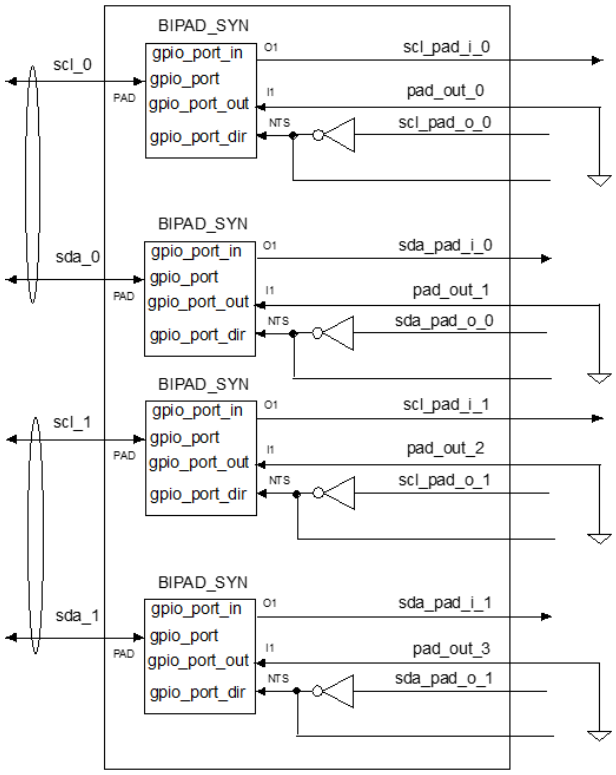
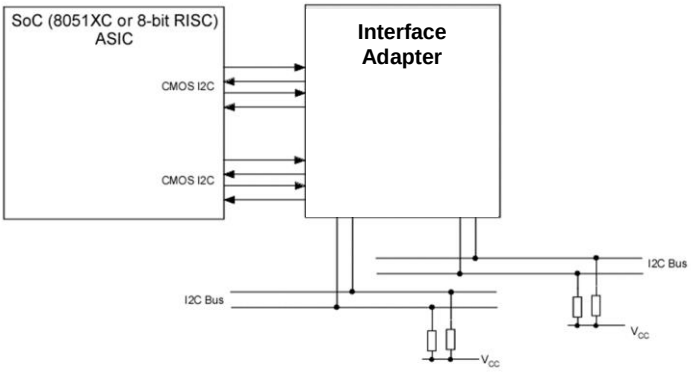
CMOS I2C to Pull-up Bus Conversion (Dual)

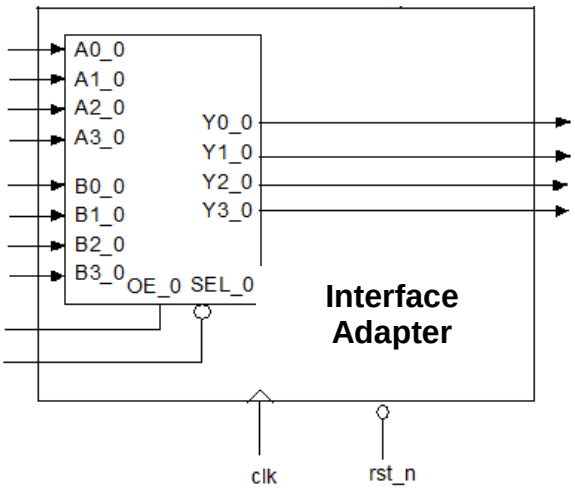




- ✓ Eliminates need for transistors for I2C CMOS to Pull-up bus conversion

74HC157 Logic Compatible Mux

- ✓ Provides on-chip 2 to 1 Mux for SPI Slave Select (Programming/Boot-up)



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